REMARKS

Claims 48-62 are pending the application. Claims 48-62 stand rejected under 35 U.S.C. §103(a) over United States patent number 5,346,838 to Ueno (Ueno) in view of United States patent number 4,861,731 to Bhagat (Bhagat). Claims 48 and 55 have been amended to more clearly define the invention.

The present application relates to forming a thyristor including a gated diode by gating a semiconductor junction with a polysilicon gate. Page 10, lines 10-15. The polysilicon gate can be biased (Page 11, line 15) to produce latch up (Page 12, line 8).

In view of the above, claim 48 recites:

> A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising the following steps: providing a semiconductor substrate; providing doped silicon regions to form a multi-region planar thyristor having at least four regions; forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode; connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor; and incorporating said multi-region planar thyristor in a memory device, said memory device adapted to store information using said latchup of said multi-region planar thyristor.

The Ueno reference relates to an "insulated gate control thyristor including an n-type base region, an insulating layer, gates formed on the insulating layer, first and second windows formed in the insulating layer, p-type emitter layers and n-type cathode layers diffused into the base region from the first windows, and p-type collector layers diffused into the base region from the second windows. The emitter layer and the collector layer are disposed in close proximity to each other under the gate so that a channel is formed which is conducted when the thyristor is turned off." Abstract.

The Office Action expressly acknowledges that Ueno does not disclose "forming at least one polysilicon gate overlying a single junction," and the combination of Ueno with Bhagat is thus proposed by the Office Action. However, Ueno and Bhagat, taken individually or in combination also do not teach or suggest "incorporating said multi-region planar thyristor in a memory device, said memory device adapted to store information using said latchup of said multi-region planar thyristor." Accordingly, the rejection of claim 48 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat is overcome.

Furthermore, Applicant continues to believe that the proposed combination of Ueno and Bhagat is not supported by the prior art. In order to combine references to support a rejection under 37 C.F.R. § 103(a) there must be found a motivation or suggestion in the prior art to make the combination.

The references now of record teach directly away from combining Bhagat with Ueno. The Ueno reference relates to a device having a semiconductor body including "a p-type substrate of a high impurity concentration functioning as an anode region 11. " Column 7, lines 30-31. This is shown in Fig. 3 as a back contact A.

In contrast, the Bhagat reference relates to a semiconductor power device. A "buried dielectric layer 22 defines electrically isolated thyristor cell 24." Column 4, lines 1-2. This structure is shown in Figures 1 and 2 in which dielectric layer 22 surrounds the balance of the Bhagat device, and isolates it from the substrate 20. The presence of the dielectric layer 22 of Bhagat precludes the use of a back contact as shown in Fig. 3 of the Ueno reference. A structure combining the features of the Bhagat and Ueno devices would be inoperative, since no back contact could be made through the Bhagat dielectric layer. This fundamental incompatibility between the Ueno and Bhagat devices teaches away from the combination suggested in the Office Action. Moreover, absent hindsight, there is no motivation found in the prior art to extract the isolated structure of the Bhagat gate and combine it with the Bhagat device. Accordingly, there is no suggestion or motivation to combine the substance of the Ueno reference with that of Bhagat. Therefore, the rejection of claim 48 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat should be withdrawn,

and claim 48 should be allowed.

Claims 49-54 each depend directly or indirectly from claim 48, and incorporate every limitation thereof. Therefore, the rejections of claims 49-54 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat are overcome for at least the same reasons given above in relation to claim 48.

Claim 55 recites "incorporating said multi-region planar thyristor in a memory device, said memory device adapted to store information using said latchup of said multi-region planar thyristor." As discussed above in relation to claim 48, Ueno and Bhagat, taken individually or in combination also do not teach or suggest "incorporating said multi-region planar thyristor in a memory device, said memory device adapted to store information using said latchup of said multi-region planar thyristor." Accordingly, the rejection of claim 55 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat is overcome.

Claims 56-61 each depend directly or indirectly from claim 55, and incorporate every limitation thereof. Therefore, the rejections of claims 56-61 under 35 U.S.C. § 103(a) over Ueno in view of Bhagat are overcome for at least the same reasons given above in relation to claim 48.

Claim 62 recites:

> A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising: providing a semiconductor substrate; providing doped silicon regions to form a multi-region planar thyristor having at least four regions; forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode; and connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor, whereby said thyristor transitions from a

first one to a second one of said at least two possible current states.

The body of claim 62 refers to the preamble thereof. Thus, claim 62 includes the limitation of "forming a circuit for storing information as one of at least two possible stable current states." Ueno and Bhagat, taken individually or in combination also do not teach or suggest "forming a circuit for storing information as one of at least two possible stable current states." Accordingly, the rejection of claim 62 under 35 U.S.C. §103(a) over Ueno in view of Bhagat should be withdrawn

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

48. (Thrice Amended) A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode; [and]

connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor; and

incorporating said multi-region planar thyristor in a memory device, said memory device adapted to store information using said latchup of said multi-region planar thyristor.

55. (Once Amended) A method of forming a device for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode, said gate adapted to receive a voltage for producing latch-up in said multi-region planar thyristor ;and

incorporating said multi-region planar thyristor in a memory device, said memory device adapted to store information using said latchup of said multi-region planar thyristor.